Remarks

Applicants respectfully request reconsideration of this application as amended. Claims 1, 15, 24 and 31 have been amended. No claims have been canceled. Therefore, claims 1-31 are now presented for examination.

Claims 1-3, 8, 10, 14-17, 21, 23-25, and 31-33 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Shimoi et al. (U.S. Patent No. 5,652,857) and Corcoran et al. (U.S. Patent No. 6,449,689). Applicants submit that the present claims are patentable over Shimoi in view of Corcoran.

Shimoi discloses a disk control apparatus for recording and reproducing compression data to physical device of direct access type. The apparatus includes a cache memory between a host computer and a disk drive. The cache memory is divided into a non-compression cache memory for storing non-compression data on a logic block unit basis and a compression cache memory for storing compression data on a compression group unit basis having the same size as that of the logic sector of the disk drive. A compressing circuit extracts the data stored in the non-compression cache memory on a logic block unit basis and compresses the data. A compression group forming unit collects the compression data of the logic block unit by the compressing circuit unit, thereby forming a compression group and storing the compression group into the compression cache memory. An expanding circuit unit extracts the data stored in the compression cache memory on a compression group unit basis, expands, and develops into the non-compression cache memory. See Shimoi at col. 3, ll. 23-65.

Corcoran discloses a system and method for organizing compressed data on a storage disk to increase storage density. The method and system include a compressor for

compressing a data block into a compressed data block, wherein N represents a compression ratio. The storage disk includes a first storage partition having N slots for storing compressed data, and a second storage partition also having N slots for storing overflow data. Each of the N slots in the first partition includes at least one address pointer for pointing to locations in the second partition. According to a further aspect of the system and method, if the compressed data block is less than or equal to 1/N of the data block size, then the compressed data block is stored in a first slot in the first storage partition. If the compressed data block is greater than 1/N of the data block size, then the first 1/N of the compressed data block is stored in the first slot in the first storage partition and a remainder of the compressed block is stored in one or more slots in the second storage partition. The address pointer in the first slot is then updated to point to the one or more slots in the second storage partition. See Corcoran at Abstract.

Claim 1 of the present application recites compression logic to form a compressed cache line by combining a retrieved cache line having a first address comprising a first companion bit value with a companion cache line having the first address comprising a second companion bit value if the companion cache line is resident in the cache memory. Applicants submit that Shimoi and Corcoran both fail to disclose or suggest such a feature. Particularly, there is no disclosure or suggestion in Shimoi of cache line having a first address comprising a first companion bit value being compressed with a companion cache line having the first address comprising a second companion bit value.

Because both Shimoi and Corcoran fail to disclose or suggest compression logic to form a compressed cache line by combining a retrieved cache line having a first address comprising a first companion bit value with a companion cache line having the first address

comprising a second companion bit value if the companion cache line is resident in the cache memory, any combination of Shimoi and Corcoran would also fail to disclose or suggest the feature. Therefore, claim 1 is patentable over Shimoi in view of Corcoran.

Claims 2-14 depend from claim 1 and include additional features. Thus, claims 2-14 are also patentable over Shimoi in view of Corcoran.

Claim 15 recites a main cache having a plurality of cache lines wherein a cache line is compressed by combining a retrieved cache line having a first address comprising a first companion bit value with a companion cache line having the first address comprising a second companion bit value if the companion cache line is resident in the cache memory. For the reasons discussed above with respect to claim 1, claim 15 is also patentable over Shimoi in view of Corcoran. Since claims 16-23 depend from claim 15 and include additional features, claims 16-23 are also patentable over Shimoi in view of Corcoran.

Claim 24 recites combining a retrieved cache line having a first address comprising a first companion bit value with a companion cache line having the first address comprising a second companion bit value if the companion cache line is resident in a main cache. Thus, for the reasons discussed above with respect to claim 1, claim 24 is also patentable over Shimoi in view of Corcoran. Because claims 25-30 depend from claim 24 and include additional features, claims 25-30 are also patentable over Shimoi in view of Corcoran.

Claim 31 recites a cache controller having compression logic to form a compressed cache line by combining a retrieved cache line with a companion cache line if the companion cache line is resident in the cache memory. Thus, for the reasons discussed above with

respect to claim 1, claim 31 is also patentable over Shimoi in view of Corcoran. Because claims 32 and 33 depend from claim 31 and include additional features, claims 32 and 33 are also patentable over Shimoi in view of Corcoran.

Claims 4-7, 9, 18-20, 22, and 26-30 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Shimoi and Corcoran as applied to claims 3, 8, 17, 21 and 25, respectively, and further in view of Obara (U.S. Patent No. 6,115,787). Applicants submit that the present claims are patentable over Shimoi and Corcoran even in view of Obara.

Obara discloses storing compressed records into a cache memory of a disk storage system in an easy-to-read manner. Data to be stored in the cache memory is divided into plural data blocks each having two cache blocks in association with track blocks to which the data belongs and are compressed. The respective data blocks after the compression are stored in one or plural cache blocks. Information for retrieving each cache block from an in-track address for the data block is stored as part of retrieval information for the cache memory. When the respective data blocks in a record is read, the cache block storing the compressed data block is determined based on the in-track address of the data block and the retrieval information. See Obara at Abstract.

However, Obara does not disclose or suggest combining a retrieved cache line having a first address comprising a first companion bit value with a companion cache line having the first address comprising a second companion bit value if the companion cache line is resident in a main cache. As discussed above, both Shimoi and Corcoran fail to disclose or suggest combining a retrieved cache line having a first address comprising a first companion bit value with a companion cache line having the first address comprising a second companion bit value if the companion cache line is resident in a main cache. Therefore, any combination

of Shimoi, Corcoran and Obara would also not disclose or suggest combining a retrieved cache line having a first address comprising a first companion bit value with a companion cache line having the first address comprising a second companion bit value if the companion cache line is resident in a main cache. As a result, the present claims are patentable over Shimoi and Corcoran in view of Obara.

Claims 11-13 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Shimoi and Corcoran as applied to claim 10 above, and further in view of Cypher (U.S. Patent No. 6,629,205). Applicants submit that the present claims are patentable over Shimoi and Corcoran even in view of Cypher.

Cypher discloses a cache memory including a plurality of memory chips that are configured to collectively store a plurality of cache lines. Each cache line includes data and an associated cache tag. The cache tag may include an address tag which identifies the line as well as state information indicating the coherency state for the line. Each cache line is stored across the memory chips in a row formed by corresponding entries (i.e., entries accessed using the same index address). The plurality of cache lines is grouped into separate subsets based on index addresses, thereby forming several separate classes of cache lines. The cache tags associated with cache lines of different classes are stored in different memory chips. During operation, the cache controller may receive multiple snoop requests corresponding to, for example, transactions initiated by various processors. The cache controller is configured to concurrently access the cache tags of multiple lines in response to the snoop requests if the lines correspond to differing classes. See Cypher at Abstract.

Nonetheless, Cypher does not disclose or suggest combining a retrieved cache line having a first address comprising a first companion bit value with a companion cache line

having the first address comprising a second companion bit value if the companion cache line is resident in a main cache. As discussed above, both Shimoi and Corcoran fail to disclose or suggest such a feature. Therefore, any combination of Shimoi, Corcoran and Cypher would also not disclose or suggest the feature. Accordingly, the present claims are patentable over Shimoi and Corcoran in view of Cypher.

Applicants respectfully submit that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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